EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	953	703/14.ccls.	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/14 08:31
S1	2	"2004/0143801"	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/10 16:40
S2	1	"20040143801"	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/10 16:41
S3	1	("6053947").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/03/10 16:43
S4	33	(generat$3 or automated) near2 testbench and (partition or submodule or module) and pin	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/10 16:46
S5	19	(generat$3 or automated) near2 testbench and (partition or submodule or module) and pin and asic and program$4	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 09:48
S6	43	(generat$3 or automated) near2 (testbench or (test near2 design))and (partition or submodule or module) and pin and asic and program$4	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 09:49
S7	25	(generat$3 or automated) near2 (test near2 design) and (partition or submodule or module) and pin and asic and program$4	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 09:50
S8	29	(generat$3 or automated) near2 (test near2 design) and (partition or submodule or module) and pin and (asic or fpga)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 15:56
S9	6	(top near2 level) and submodule and interface and input and output and (test design)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 16:16
S10	2	(("6477691") or ("6377581")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/03/13 17:07
S11	13660	input and output and ((clock and control and data) near2 (line or bus))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:08
S12	0	S11 and (adder and register and phase lock loop and memory and timer) and (sychronous and asynchronous) and (testbench or (test design))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:09

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S13	0	S11 and (adder and register and phase lock loop and memory and timer) and (sychronous and asynchronous)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:09
S14	0	S11 and (adder and register and timer) and (sychronous and asynchronous)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:09
S15	11	S11 and (sychronous and asynchronous)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/14 08:31
S16	636	S11 and (adder and timer and phase)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:11
S17	617	S11 and (adder and timer and phase and memory)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:11
S18	243	S11 and (adder and timer and phase lock and memory)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:11
S19	240	S11 and (adder and timer and phase lock loop and memory)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:11
S20	0	S11 and (adder and timer and phase lock loop and memory) and testbench	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:12
S21	112	S11 and (adder and timer and phase lock loop and memory) and simulat$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:13
S22	0	S11 and (adder and timer and phase lock loop and memory) and simulat$3 and (test with design)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:12
S23	142	S11 and (adder and timer and pll and memory) and simulat$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/03/13 17:14